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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 3

Application Number	09/805,843
Filing Date	March 13, 2001
First Named Inventor	Edward Aung
Art Unit	2638
Examiner Name	Emmanuel Bayard
Attorney Docket Number	174/183
Confirmation Number	3795



## U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
EB		4,229,825	10/21/1980	Guidoux	
		4,680,779	07/14/1987	Wakerly	
		5,034,967	07/23/1991	Cox et al.	
		5,084,891	01/28/1992	Ariyavisitakul et al.	
		5,162,762	11/10/1992	Flanagan	
		5,184,350	02/02/1993	Dara	
		5,357,249	10/18/1994	Azaren et al.	
		5,457,717	10/10/1995	Bellamy	
		5,481,563	01/02/1996	Hamre	
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		5,781,038	07/14/1998	Ramamurthy et al.	
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		6,266,799 B1	07/24/2001	Lee et al.	
EB		6,295,563 B1	09/25/2001	Whittaker	

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		Number-Kind Code <sup>2</sup> (if known)			
EB		6,327,196 B1	12/04/2001	Mullarkey	
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EB					

## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
EB		JP 04287439 A	10/13/1992	Fujitsu Ltd.		
EB		JP 05199107 A	08/06/1993	Hitachi Ltd Hitachi Comput Eng Corp. Ltd.		
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**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	
EB		Charles R. Hogge, Jr., "A Self Correcting Clock Recovery Circuit," IEEE Transactions On Electron Devices, Vol. ED-32, No. 12, pp. 2704-2706, December 1985.
		Timothy H. Hu et al., "A Monolithic 480 Mb/s parallel AGC/Decision/Clock-Recovery Circuit in 1.2- $\mu$ m CMOS," IEEE Journal Of Solid-State Circuits, Vol. 28, No. 12, December 1993.
		Ilya I. Novof et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and $\pm 50$ ps Jitter," IEEE Journal Of Solid-State Circuits, Vol. 30, No. 11, pp. 1259-1266, November 1995.
		Ricardo Monleone, "Clock-recovery PLL fits into single PLD," EDN, pp. 88-92, November 23, 1995.
		Fong, Thomas Kin Tak, "Advanced clock recovery techniques for high-speed packet-switched optical networks," ProQuest, Abstract (Document Summary), 1995.
		M. Rau, et al., "Clock/Data Recovery PLL Using Half-Frequency Clock," IEEE Journal Of Solid-State Circuits, Vol. 32, No. 7, July 1997.
↓		German Gutierrez et al., "Unaided 2.5 Gb/s Silicon Bipolar Clock and Data Recovery IC," IEEE Radio Frequency Integrated Circuits Symposium, VIII-7, pp. 173-176, 1998.
EB		Ankit Seedher et al., "Fractional Rate Phase Detectors for Clock and Data Recovery," IEEE, pp. 313-316, 2003.

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